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EXAMINER	
GOLDEN, JAMES R	

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2187	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 10/699,318	Applicant(s) COCHRAN ET AL.	
	Examiner James Golden	Art Unit 2187	

-- *The MAILING DATE of this communication appears on the cover sheet with the correspondence address* --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 October 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-26* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-26* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☒ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *10/30/2003*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

The instant application 10/699318 has a total of 26 claims pending. There are 4 independent claims and 22 dependent claims. Claims 1-26 have been rejected in view of prior art.

Oath/Declaration

1. The oath or declaration is defective. A new oath or declaration in compliance with 37 CFR 1.67(a) identifying this application by application number and filing date is required. See MPEP §§ 602.01 and 602.02.

2. The oath or declaration is defective because characters are missing from the residence and post office city of the first applicant, and from the name of the second applicant.

Information Disclosure Statement

3. The information disclosure statement submitted on 10/30/2003 is in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statement is being considered by the examiner.

Drawings

4. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they do not include the following reference sign mentioned in the description: 600 of Fig. 6 [0035, line 3]. Also, the ranges "420a-426a" and "420b-426b"

of Fig. 4 [0029, lines 2-3] include reference signs not present in the drawings, so these should be corrected to read --420a, 422a, 424a and 426a-- and --420b, 422b, 424b and 426b--.

5. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they include the following reference character(s) not mentioned in the description: 718 of Fig. 6 [0044, line 9]. This should most likely be corrected to read --618--.

6. Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Specification

7. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed. The title "Determination of Optimal Block Size for Copy Operations" is suggested.

Claim Objections

8. **Claims 20-25** are objected to because they recite the limitation "the network element" in line 1. There is insufficient antecedent basis for this limitation in the claim. These objections could be overcome by correcting line 3 of claim 19 to read --a network element--, or line 1 of claims 20-25 to read --the network interface--.

Claim Rejections - 35 USC § 102

9. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

10. **Claims 1-3, 8-10, 13 and 15-18** are rejected under 35 U.S.C. 102(e) as being anticipated by Begis et al. (US 6,678,812).

11. **With respect to claim 1**, Begis et al. disclose a method, comprising:

- initiating a copy operation from a first storage cell to a second storage cell, wherein the copy operation initially utilizes a first write block size (column 1, lines 14-16; column 4, lines 35-37; the read operation copies data from a data cell in a hard drive to a data cell on the processor);
- changing the write block size to utilize a second write block size, different from the first write block size (column 4, lines 53-54);
- measuring a performance parameter at the second write block size (column 4, lines 4-15, lines 38-43, lines 53-54; the throughput is measured for the first transfer block size, and the process is repeated for the second and subsequent transfer block sizes); and
- maintaining the second block size if the performance parameter exceeds a threshold (column 4, lines 57-59; the transfer block size with the highest throughput is selected, so if the last transfer block size has a throughput that exceeds the throughput of the next fastest transfer block size, it is maintained).

12. **With respect to claim 2**, Begis et al. disclose the method of claim 1 (see above paragraph 11), wherein initiating a copy operation from a first storage cell to a second storage cell comprises setting the first write block size to a lower bound of write block sizes (column 2, lines 4-7, lines 11-12; a number of transfer block sizes are examined which inherently include a smallest size, i.e. a lower bound).

13. **With respect to claim 3**, Begis et al. disclose the method of claim 2 (see above paragraph 12), further comprising measuring a performance parameter at the first write block size (column 4, lines 4-15, lines 38-43).

14. **With respect to claim 8**, Begis et al. disclose a method, comprising

- initiating a data transfer operation between a first storage cell and a second storage cell, wherein the data transfer operation initially utilizes a write block size referred to as a native write block size (column 1, lines 14-16; column 4, lines 35-37; the read operation transfers data from a data cell in a hard drive to a data cell on the processor, where the first transfer block size is considered the native write block size);
- determining a data transfer performance parameter associated with the native write block size (column 4, lines 4-15, lines 38-43);
- varying the write block size through a plurality of write block sizes different than the native write block size (column 2, lines 4-7, lines 11-12);
- determining a data transfer performance parameter associated with at least one of the plurality of write block sizes different than the native write block size (column 4, lines 4-15, lines 38-43, lines 53-54; the throughput is measured for the first transfer block size, and the process is repeated for the second and subsequent transfer block sizes); and
- changing the native write block size if the data transfer performance parameter at one of the plurality of write block sizes different than the native write block size satisfies a performance threshold (column 4, lines 53-65).

15. **With respect to claim 9**, Begis et al. disclose the method of claim 8 (see above paragraph 14), further comprising establishing one or more parameters pursuant to

which the data transfer operation is initiated (column 3, line 51 -- column 4, line 3; parameters are set before optimization begins).

16. **With respect to claim 10**, Begis et al. disclose the method of claim 8 (see above paragraph 14), wherein varying the write block size through a plurality of write block sizes different than the native write block size comprises

- setting the write block size to a first write block size (column 4, lines 30-35); and
- changing the write block size in response to a triggering event (column 4, lines 51-54).

17. **With respect to claim 13**, Begis et al. disclose the method of claim 8 (see above paragraph 14), wherein determining a data transfer performance parameter associated with the native write block size comprises measuring a data transmission throughput at the native write block size (column 4, lines 8-11, lines 38-43).

18. **With respect to claim 15**, Begis et al. disclose the method of claim 8 (see above paragraph 14), wherein determining a performance parameter associated with at least one of the plurality of write block sizes different than the native write block size further comprises:

- recording a data transfer performance parameter at at least one write block size in a memory location (122 of Fig. 4; column 4, lines 4-6); and
- associating the data transmission performance parameter with the write block size (122 of Fig. 4; column 4, lines 8-11).

19. **With respect to claim 16**, Begis et al. disclose the method of claim 8 (see above paragraph 14), wherein changing the native write block size if the data transfer

performance parameter at one of the plurality of write block sizes different than the native write block sizes satisfies a performance threshold comprises changing the native write block size if the data transfer performance parameter at one of the plurality of write block sizes different than the native write block size is greater than the corresponding performance parameter at the native write block size (Fig. 6; column 4, lines 53-65).

20. **With respect to claim 17**, Begis et al. disclose the method of claim 8 (see above paragraph 14), further comprising:

- recording, in a suitable memory location, an array of performance parameters associated with write block sizes (122 of Fig. 4; column 4, lines 4-6, lines 8-11);
- searching the array for the best performance parameter (240 of Fig. 5; column 4, lines 57-65); and
- changing the native block size to the block size associated with the best performance parameter (240 of Fig. 5; column 4, lines 57-59).

21. **With respect to claim 18**, Begis et al. disclose a computer program product comprising logic instructions recorded on a computer-readable medium that, when executed cause a computer to execute the method of claim 8 (column 2, lines 61-63; see above paragraph 16).

Claim Rejections - 35 USC § 103

22. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

23. **Claims 4-7 and 11** are rejected under 35 U.S.C. 103(a) as being unpatentable over Begis et al. (US 6,678,812) as applied to claims 1-3, 8-10, 13 and 15-18 above, and further in view of Yen et al. (US 2004/0071166).

24. **With respect to claim 4**, Begis et al. disclose the method of claim 3 (see above paragraph 13). Begis et al. do not disclose the limitation wherein changing the write block size to utilize a second write block size, different from the first write block size, comprises incrementing the write block size.

However, Yen et al. disclose the limitation wherein changing the write block size to utilize a second write block size, different from the first write block size, comprises incrementing the write block size (Tables 2-4) [0030-0032; the packet sizes start at 64 bytes, a lower bound, and are incremented to 71 bytes].

Begis et al. and Yen et al. are analogous art because they are from the same field of endeavor, namely the determination of optimal packet sizes.

At the time of invention, it would have been obvious to a person of ordinary skill in the art to combine the incrementing of packet sizes of Yen et al. with the varied transfer block sizes of Begis et al. in determining the optimal transfer block size. The motivation for doing so would have been because it "allows the IPG [inter-packet gap] generator to provide an IPG that take into account varying combinations of packet sizes" [0033, lines 2-3].

Therefore, it would have been obvious to a person of ordinary skill in the art to combine Yen et al. with Begis et al. for the benefit of a method for determining the optimal transfer block size that varies the packet size by incrementing to obtain the invention as specified in claim 4.

25. **With respect to claim 5**, Begis et al. and Yen et al. disclose the method of claim 4 (see above paragraph 24), wherein maintaining the second block size if the performance parameter exceeds a threshold comprises comparing the performance parameter measured at the first block size with the performance parameter measured at the second block size (Fig. 6; column 4, lines 57-65).

26. **With respect to claim 6**, Begis et al. and Yen et al. disclose the method of claim 5 (see above paragraph 25), further comprising repeatedly incrementing the write block size and comparing a performance parameter at a current write block size with a performance parameter at a previous write block size (column 4, lines 53-65; if the last transfer block size examined is considered the current transfer block size, then its throughput is compared to the measured throughput of previous transfer block sizes).

27. **With respect to claim 7**, Begis et al. and Yen et al. disclose the method of claim 5 (see above paragraph 26), further comprising terminating incrementing the write block size when the current write block size reaches an upper bound (column 2, lines 11-12; column 4, lines 54-57).

28. **With respect to claim 11**, Begis et al. and Yen et al. disclose the method of claim 10 (see above paragraph 16). Begis et al. do not disclose the limitation wherein

the first write block size is a lower bound of a range of write block sizes and changing the write block size comprises increasing the write block size by a defined increment.

However, Yen et al. disclose the limitation wherein the first write block size is a lower bound of a range of write block sizes and changing the write block size comprises increasing the write block size by a defined increment (Tables 2-4) [0030-0032; the packet sizes start at 64 bytes, a lower bound, and are incremented to 71 bytes].

Begis et al. and Yen et al. are analogous art because they are from the same field of endeavor, namely the determination of optimal packet sizes.

At the time of invention, it would have been obvious to a person of ordinary skill in the art to combine the incrementing of packet sizes of Yen et al. with the varied transfer block sizes of Begis et al. in determining the optimal transfer block size. The motivation for doing so would have been because it "allows the IPG [inter-packet gap] generator to provide an IPG that take into account varying combinations of packet sizes" [0033, lines 2-3].

Therefore, it would have been obvious to a person of ordinary skill in the art to combine Yen et al. with Begis et al. for the benefit of a method for determining the optimal transfer block size that varies the packet size by incrementing to obtain the invention as specified in claim 11.

29. **Claim 12** is rejected under 35 U.S.C. 103(a) as being anticipated over Begis et al. (US 6,678,812) as applied to claims 1-3, 8-10, 13 and 15-18 above, and further in view of in view of James et al. (US 6,006,289).

30. **With respect to claim 12**, Begis et al. disclose the method of claim 10 (see above paragraph 16). Begis et al. do not disclose the limitation wherein the first write block size is an upper bound of a range of write block sizes and changing the write block size comprises increasing the write block size by a defined increment.

However, James et al. disclose the limitation wherein the first write block size is an upper bound of a range of write block sizes and changing the write block size comprises increasing the write block size by a defined increment (571 of Fig. 5A; column 9, lines 34-37; since the block size is only decremented, it must start from an upper bound).

Begis et al. and James et al. are analogous art because they are from the same field of endeavor, namely the determination of optimal packet sizes.

At the time of invention, it would have been obvious to a person of ordinary skill in the art to combine the decrementing of data block sizes of James et al. with the varied transfer block sizes of Begis et al. in determining the optimal transfer block size. The motivation for doing so would have been because "the target lacks buffer capacity to receive the data block" (column 9, lines 34-36) and it may have buffer capacity for a data block of smaller size.

Therefore, it would have been obvious to a person of ordinary skill in the art to combine James et al. with Begis et al. for the benefit of a method for determining the optimal transfer block size that varies the packet size by decrementing to obtain the invention as specified in claim 12.

31. **Claims 14, 19 and 21-26** are rejected under 35 U.S.C. 103(a) as being anticipated over Begis et al. (US 6,678,812) as applied to claims 1-3, 8-10, 13 and 15-18 above, and further in view of in view of Bournas (US 6,769,030).

32. **With respect to claim 14**, Begis et al. disclose the method of claim 8 (see above paragraph 14). Begis et al. do not disclose the limitation wherein determining a data transfer performance parameter associated with the native write block size comprises measuring a round trip transmission time at the native write block size.

However, Bournas discloses the limitation wherein determining a data transfer performance parameter associated with the native write block size comprises measuring a round trip transmission time at the native write block size (column 3, lines 65-66).

Begis et al. and Bournas are analogous art because they are from the same field of endeavor, namely the determination of optimal transfer block sizes.

At the time of invention, it would have been obvious to a person of ordinary skill in the art to combine the round trip transmission time parameter of Bournas with the throughput parameter of Begis et al. in determining the optimal transfer block size. The motivation for doing so would have been because "an average round trip... [is] used to calculate the optimal network packet size" (column 3, line 65 -- column 4, line 1).

Therefore, it would have been obvious to a person of ordinary skill in the art to combine Bournas with Begis et al. for the benefit of a method for determining the optimal transfer block size that takes into account round trip transmission time as well as throughput to obtain the invention as specified in claim 14.

33. **With respect to claim 19**, Begis et al disclose a network element in a computer-based storage network, comprising:

- a processor (14 of Fig. 1; column 2, line 58);
- a memory module (18 of Fig. 1; column 2, lines 58-59); and
- a communication bus that provides a communication connection between the processor and the memory module (28 of Fig. 1; column 2, line 64),
- wherein the memory module comprises logic instructions (column 2, lines 61-63) that, when executed on the processor, cause the processor to:
    - initiate a data transfer operation between a first storage cell and a second storage cell, wherein the data transfer operation initially utilizes a write block size referred to as a native write block size (column 1, lines 14-16; column 4, lines 35-37; the read operation transfers data from a data cell in a hard drive to a data cell on the processor, where the first transfer block size is considered the native write block size);
    - determine a data transfer performance parameter associated with the native write block size (column 4, lines 4-15, lines 38-43);
    - periodically vary the write block size through a plurality of write block sizes different than the native write block size (column 2, lines 4-7, lines 11-12);
    - determine a data transfer performance parameter associated with at least one of the plurality of write block sizes different than the native write block size (column 4, lines 4-15, lines 38-43, lines 53-54; the throughput is

measured for the first transfer block size, and the process is repeated for the second and subsequent transfer block sizes); and

- change the native write block size if the data transfer performance parameter at one of the plurality of write block sizes different than the native write block size satisfies a performance threshold (column 4, lines 53-65).

Begis et al. do not disclose the limitations wherein the network comprises:

- a network interface;
- a communication bus that provides a communication connection between the network interface, the processor, and the memory module.

However, Bournas discloses the limitations wherein the network comprises:

- a network interface (210 of Fig. 2; column 3, lines 31-34);
- a communication bus that provides a communication connection between the network interface, the processor, and the memory module (206 of Fig. 2; column 3, lines 31-34).

Begis et al. and Bournas are analogous art because they are from the same field of endeavor, namely the determination of optimal transfer block sizes.

At the time of invention, it would have been obvious to a person of ordinary skill in the art to combine the bus with a network adapter of Bournas with the bus of Begis et al. The motivation for doing so would have been because "In high-speed network 116, the transmission of data is broken into cells of equal size. The present invention recognizes that in this situation, the IP packet size is not limited to a maximum size.

This flexibility in choosing the network packet size allows for much higher file transfer rates to be achieved when an optimal packet size is selected" (column 2, lines 53-58). Data packets could be transferred not only from a hard drive to the processor as in Begis et al., but between different computers on the network through the network adapter.

Therefore, it would have been obvious to a person of ordinary skill in the art to combine Bournas with Begis et al. for the benefit of a packet-optimizing device that allows packets to be transferred between computers on the network to obtain the invention as specified in claim 19.

34. **With respect to claim 21**, Bournas and Begis et al. disclose the network element of claim 19 (see above paragraph 33), wherein the logic instructions that cause the network element to determine a data transfer performance parameter associated with the native write block size further cause the network element to measure a data transmission throughput at the native write block size (column 4, lines 8-11, lines 38-43).

35. **With respect to claim 22**, Bournas and Begis et al. disclose the network element of claim 19 (see above paragraph 33). Begis et al. disclose the limitations wherein the logic instructions that cause the network element to determine a data transfer performance parameter associated with the native write block size further cause the network element to measure a round trip transmission time at the native write block size (see above paragraph 32).

36. **With respect to claim 23**, Bournas and Begis et al. disclose the network element of claim 19 (see above paragraph 33). Begis et al. disclose the limitations wherein the logic instructions that cause the network element to determine a data transfer performance parameter associated with at least one of the plurality of write block sizes different than the native write block size further cause the network element to:

- record a data transfer performance parameter at a plurality of write block sizes in a memory location (122 of Fig. 4; column 4, lines 4-6); and
- associate the data transmission performance parameter with the write block size (122 of Fig. 4; column 4, lines 8-11).

37. **With respect to claim 24**, Bournas and Begis et al. disclose the network element of claim 19 (see above paragraph 33). Begis et al. disclose the limitations wherein the logic instructions that cause the network element to change the native block size if the data transfer performance parameter at one of the plurality of write block sizes different than the native write block sizes satisfies a performance threshold further cause the network element to change the native write block size if the data transfer performance parameter at one of the plurality of write block sizes different than the native write block size is greater than the corresponding performance parameter at the native write block size (Fig. 6; column 4, lines 53-65).

38. **With respect to claim 25**, Bournas and Begis et al. disclose the network element of claim 19 (see above paragraph 33). Begis et al. disclose the limitations wherein the logic instructions that cause the network element to:

- record, in a suitable memory location, an array of performance parameters associated with write block sizes (122 of Fig. 4; column 4, lines 4-6, lines 8-11);
- search the array for the best performance parameter (240 of Fig. 5; column 4, lines 57-65); and
- change the native block size to the block size associated with the best performance parameter (240 of Fig. 5; column 4, lines 57-59).

39. **With respect to claim 26**, Begis et al disclose a network element in a computer-based storage network, comprising:

- a processor (14 of Fig. 1; column 2, line 58);
- a memory module (18 of Fig. 1; column 2, lines 58-59); and
- a communication bus that provides a communication connection between the processor and the memory module (28 of Fig. 1; column 2, line 64),
- means for initiating a data transfer operation between a first storage cell and a second storage cell, wherein the data transfer operation initially utilizes a write block size referred to as a native write block size (column 1, lines 14-16; column 4, lines 35-37; the read operation transfers data from a data cell in a hard drive to a data cell on the processor, where the first transfer block size is considered the native write block size);
- means for determining a data transfer performance parameter associated with the native write block size (column 4, lines 4-15, lines 38-43);

At the time of invention, it would have been obvious to a person of ordinary skill in the art to combine the bus with a network adapter of Bournas with the bus of Begis et al. The motivation for doing so would have been because "In high-speed network 116, the transmission of data is broken into cells of equal size. The present invention recognizes that in this situation, the IP packet size is not limited to a maximum size. This flexibility in choosing the network packet size allows for much higher file transfer rates to be achieved when an optimal packet size is selected" (column 2, lines 53-58). Data packets could be transferred not only from a hard drive to the processor as in Begis et al., but between different computers on the network.

Therefore, it would have been obvious to a person of ordinary skill in the art to combine Bournas with Begis et al. for the benefit of a packet-optimizing device that allows packets to be transferred between computers on the network to obtain the invention as specified in claim 26.

40. **Claim 20** is rejected under 35 U.S.C. 103(a) as being unpatentable over Begis et al. (US 6,678,812) in view of Bournas (US 6,769,030) as applied to claims 14, 19 and 21- 26 above, and still further in view of Yen et al. (US 2004/0071166).

4/2/06

41. **With respect to claim 20**, Begis et al. in view of Bournas discloses the network element of claim 19 (see above paragraph 33). Begis et al. disclose the limitations wherein the logic instructions that cause the network element to periodically vary the write block size through a plurality of write block sizes different than the native write block size further cause the network element to set the write block to a boundary write block size (column 2, lines 4-7, lines 11-12; a number of transfer block sizes are

- means for periodically varying the write block size through a plurality of write block sizes different than the native write block size (column 2, lines 4-7, lines 11-12);
- means for determining a data transfer performance parameter associated with at least one of the plurality of write block sizes different than the native write block size (column 4, lines 4-15, lines 38-43, lines 53-54; the throughput is measured for the first transfer block size, and the process is repeated for the second and subsequent transfer block sizes); and
- means for changing the native write block size if the data transfer performance parameter at one of the plurality of write block sizes different than the native write block size satisfies a performance threshold (column 4, lines 53-65).

Begis et al. do not disclose the limitations wherein the network comprises:

- a network interface;
- a communication bus that provides a communication connection between the network interface, the processor, and the memory module.

However, Bournas discloses the limitations wherein the network comprises:

- a network interface (210 of Fig. 2; column 3, lines 31-34);
- a communication bus that provides a communication connection between the network interface, the processor, and the memory module (206 of Fig. 2; column 3, lines 31-34).

Begis et al. and Bournas are analogous art because they are from the same field of endeavor, namely the determination of optimal transfer block sizes.

examined, which includes inherently a first size). Begis et al. do not disclose the limitation wherein the logic instructions cause the network element to periodically increment the write block size.

However, Yen et al. disclose the limitation wherein the logic instructions cause the network element to periodically increment the write block size (Tables 2-4) [0030-0032; the packet sizes start at 64 bytes, a lower bound, and are incremented to 71 bytes].

Begis et al. and Yen et al. are analogous art because they are from the same field of endeavor, namely the determination of optimal packet sizes.

At the time of invention, it would have been obvious to a person of ordinary skill in the art to combine the incrementing of packet sizes of Yen et al. with the varied transfer block sizes of Begis et al. in determining the optimal transfer block size. The motivation for doing so would have been because it "allows the IPG [inter-packet gap] generator to provide an IPG that take into account varying combinations of packet sizes" [0033, lines 2-3].

Therefore, it would have been obvious to a person of ordinary skill in the art to combine Yen et al. with Begis et al. for the benefit of a method for determining the optimal transfer block size that varies the packet size by incrementing to obtain the invention as specified in claim 20.

Conclusion

42. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

- McKee et al. (US 5,477,531) discloses using varying packet sizes to test network properties.
- Bahadiroglu (US 2002/0186660) discloses using network properties to calculate an optimum packet size.
- Ono (US 2001/0115956) also discloses using network properties to calculate an optimum packet size.
- Tamboli et al. ("Determination of the Optimum Packet Length and Buffer Sizes...") disclose determining optimum packet lengths for a particular network.

43. Any inquiry concerning this communication or earlier communications from the examiner should be directed to James Golden whose telephone number is 571-272-5628. The examiner can normally be reached on Monday-Friday, 8:30 AM - 5:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Donald Sparks can be reached on 571-272-4201. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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January 3, 2006

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